



further comprises a select control circuit, the select control circuit receives input information and controls the first and second switches.

- [c9] The integrated circuit of claim 8 wherein the input information comprises addressing information.
- [c10] The integrated circuit of claim 8 wherein the input information comprises the least significant bit of the address.
- [c11] The integrated circuit of claim 3 wherein the reference voltage selection circuit further comprises a select control circuit, the select control circuit receives input information and causes the reference selection circuit to generate the first or second reference voltage.
- [c12] The integrated circuit of claim 11 wherein the input information comprises addressing information.
- [c13] The integrated circuit of claim 11 wherein the input information comprises the least significant bit of the address.
- [c14] The integrated circuit of claim 1 wherein the reference voltage selection circuit comprises a first reference generator for generating the first reference voltage and a second reference voltage generator for generating the second reference voltage.
- [c15] The integrated circuit of claim 14 further comprises:  
a first switch, the first switch selectively couples the first reference generator to the sense amplifier to provide the sense amplifier with the first reference voltage; and  
a second switch, the second switch selectively couples the second reference generator to the sense amplifier to provide the sense amplifier with second reference voltage.
- [c16] The integrated circuit of claim 15 wherein the first and second switches are transistors.
- [c17] The integrated circuit of claim 16 wherein the reference voltage selection circuit

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